CS 2160 Additional Questions for Final

319. The two kinds of locality upon which caching is based are (374)

**A. Temporal and spatial**

B. Virtual and physical

C. Logical and physical

D. Charmed and strange

320. Memory in the hierarchy as it moves away from the CPU becomes (375)

A. Faster and larger

**B. Slower and larger**

C. Cheaper and larger

D. Faster and cheaper

321. The overall name for the structure and arrangement of different capabilities of memory to provide good performance at low cost is called the (375)

A. Spatial locality

B. Disk cache

**C. Memory hierarchy**

D. Memory bus

322. The miss rate is (376)

**A. how often a requested data item is not in cache memory.**

B. How often the CPU produces the wrong answer

C. The proportion of unmarried females in the population.

D. The amount of time it takes to request data from lower level cache

323. The time required to check cache tags is included in (376)

**A. Hit time**

B. Hit rate

C. Miss time

D. Miss Rate

324. Knowledge of cache parameters is useful to the compiler (377)

**A. T**

B. F

325. Which of these memory types is the slowest? (378)

A. SRAM

B. Flash

C. DRAM

**D. Magnetic**

326. Because of its size and expense, most Static RAM is not located on the CPU itself (379)

A. T

**B. F**

327. Wear leveling is used in (381)

A. Prewashed Levis

**B. Flash memory**

C. Static RAM

D. Dynamic RAM

328. The two major components to disk access time are (383)

A. Startup time and seek time

B. Rotational and translational latency

C. Hide time and seek time

**D. Rotational latency and seek time**

329. If a location in memory is mapped to one and only one block in cache, what kind of block scheme is being used? (383)

A. N-way associative

**B. Direct-mapped**

C. Tag-associated

D. Fully associative

330. If a direct-mapped cache has eight blocks, how many address bits are used to determine the block number? (385)

A. Two

**B. Three**

C. Eight

D. Four

331. Direct-mapped cache is \_\_\_ -way set associative. (385)

**A. 1**

B. 0

C. 2

D. 4

332. In a direct-mapped cache, multiple memory locations may be mapped to a single block of cache. How do we determine if the contents of the block include the memory location we're interested in? (386)

A. The block index.

B. The Page index.

**C. The cache tag.**

D. Valid bit

333. Increasing block size generally lowers the miss rate because of spatial locality. Why would increasing the block size eventually increase the miss rate? (391)

A. It takes longer to service misses on larger blocks

B. Spatial locality only goes so far

**C. With fixed cache size, the number of blocks would decrease.**

D. Temporal locality takes over

334. Sensing when the requested data word is in cache and not waiting until the entire requested block is in cache is the basis for (392)

A. Critical word first

B. Short blocking

**C. Early Restart**

D. Reordering

335. The two methods of updating memory from cache are (394)

A. read-write and read-only

B. Write-in and write-out

C. write-first and write-last

**D. Write-through and write-back**

336. Which is not a component in calculating CPU time for a program (399)

A. Clock cycle time

**B. Exception rate**

C. CPU execution cycles

D. Memory stall cycles

337. Hit time is important in calculating memory miss stall time (399)

**A. T**

B. F

338. Memory stalls are a product of (399)

A. Cache hits.

B. Processor exceptions.

C. Bus contention.

**D. Cache misses**

339. Direct-mapped cache (402)

A. Is slow, but efficient is use of space.

B. Is slow and inefficient in use of space.

C. Is fast and efficient is use of space.

**D. Is fast, but wasteful of space.**

340. Which is not a cache block scheme? (403)

A. Fully associative

**B. Coherent**

C. N-way Associative

D. Direct mapped

341. Which cache block scheme provides the most efficient use of cache blocks? (404)

A. N-way Associative

**B. Fully associative**

C. Direct mapped

D. Coherent

342. Which cache block scheme provides the fastest way of locating cache blocks? (404)

A. Coherent

**B. Direct mapped**

C. Fully associative

D. N-way Associative

343. In calculating the cache tag from an address, if the block size is 64 bytes and the cache is fully associative, how many bits right to you shift the address? (408)

A. 4

B. 8

C. 10

**D. 6**

344. For a cache composed of 64-byte blocks arranged in 16 sets of four-blocks each, how many bits right do you shift the address to obtain the cache tag? (408)

A. 6

**B. 10**

C. 8

D. 4

345. The most common strategy for replacing blocks is (408)

A. Random

B. First in first out

C. Most recently used

**D. Least Recently Used**

346. L1 and L2 cache are examples of (411)

A. Collocation of data

B. A compiler optimization

C. Cache coherency

**D. Multilevel cache**

347. Understanding cache structure allows compilers to (413)

**A. Arrange data optimally**

B. Optimize write-back

C. Compress data optimally

D. Arrange instructions optimally

348. When discussing failures, alternation between two states is important. What are these states? (418)

A. Success and failure

B. Failure and repair

C. Innage and outage

**D. Service accomplishment and service interruption**

349. A typical disk drive has a 1-million-hour mean time to fail (MTTF). In a cloud computing environment where 100,000 disks are used, how many disks would be expected to fail in a year (=8760 hours)? (419)

A. 77

**B. 876**

C. 512

D. 8

350. Availability is defined as MTTF/(MTTF + MTTR). What is the theoretical maximum availability (419)

A. infinite (=unbounded)

B. 0

C. 100

**D. 1**

351. Availability can be increased by increasing MTTF. What else can increase availability? (419)

A. Not using the system.

**B. Reducing MTTR**

C. Typing more gently on the keyboard.

D. Running only trusted applications.

352. Which is not a way of improving MTTF? (419)

A. Fault forecasting.

B. Fault avoidance.

C. Fault tolerance.

**D. Fault finding.**

353. The binary byte 00111110 if written to memory with even parity would be represented as (420)

A. 100111110

B. 000111110

C. 001111100

**D. 001111101**

354. A single parity bit can detect if two bits in a byte are inverted (420)

**A. F**

B. T

355. If a 32-bit word contains Hamming Error Correction, which bits will contain parity information? (note that the word will be longer than 32 bits) (421)

**A. 1, 2, 4, 8, 16, 32**

B. Odd-numbered bits

C. 0, 8, and 32

D. 2, 4, 6, 8, 10, 12, 14

356. In Hamming ECC code, each data bit is covered by at least two parity bits (421)

**A. T**

B. F

357. How many parity bits are the minimum needed to cover 32 bits of data with Hamming ECC? (423)

A. 8

B. 5

C. 7

**D. 6**

358. Which is not a reason for the recent resurgence of virtual machines? (424)

A. Cloud infrastructure.

B. Increasing importance of security.

**C. Global warming.**

D. Security failures and holes in operating systems.

359. In terms of lines of code, how big is a Virtual Machine Monitor compared to an operating system? (424)

A. It depends on the VMM

**B. Much smaller**

C. Much larger

D. About the same size

360. Virtual Machine Managers have almost no overhead for single-user, processor-bound applications. (425)

**A. T**

B. F

361. To be able to implement a virtual machine, the processor must have at least \_\_\_ modes (426)

A. 3 (user, kernel, supervisor)

B. 1 (user)

**C. 2 (user, kernel)**

D. 4 (user, kernel, supervisor, hypervisor)

362. An architecture which allows a virtual machine to run directly on the hardware (like the IBM 370) is called (426)

A. Golden

B. Supported

C. Platformed

**D. Virtualizable**

363. The industry leader in producing hardware on which virtual machines can run is (427)

**A. IBM**

B. VMware

C. HP

D. Intel

364. Using main memory as a cache for secondary storage is a description of (428)

A. Cache

**B. Virtual memory**

C. Logical memory

D. Physical memory

365. The virtual memory equivalent of a cache miss is (428)

A. A parity error

**B. A page fault.**

C. A disk error

D. An I/O request.

366. The purpose of virtual memory is to (428)

A. Virtualize the hardware.

**B. Make a program "think" it has more memory space than the machine has.**

C. Allow a program's running status to be monitored

D. Help the program run faster.

367. The process of finding the physical address where data specified by a virtual address is stored is called (429)

A. Bit conversion.

**B. Address translation.**

C. Physical lookup.

D. Virtual lookup.

368. The equivalent of a cache block in virtual memory is (429)

A. A table.

**B. A page.**

C. A lookup.

D. A sector.

369. Which of the following is closely related to the page size (429)

A. The difference in lengths of the virtual and physical addresses.

B. The size of the page table.

C. The number of TLB entries.

**D. The number of bits in the page offset.**

370. Address translation affects the page number as well as the page offset (430)

**A. F**

B. T

371. Originally, virtual memory was devised to fit large programs into small amounts of physical memory. Now virtual memory allows multiple virtual machines to share the same physical memory. (431)

A. F

**B. T**

372. Since page faults are negligible in their service time, algorithms concerned with page replacement can be simple and fast (432)

**A. F**

B. T

373. What data structure provides the information to translate a virtual address to a physical address (432)

**A. A page table**

B. A register file

C. A cache

D. The disk cache

374. The program counter, register contents, and page table constitute (432)

A. The threads of a process.

**B. The process state.**

C. The translation lookaside buffer.

D. The instruction cache.

375. When translating from a virtual address to a physical address, which does not change? (433)

A. The physical page number

B. The translation lookaside buffer

**C. The page offset**

D. The virtual page number

376. Whereas least recently used (LRU) is one of several schemes used for cache block replacement, virtual memory management uses LRU exclusively (434)

A. F

**B. T**

377. What is a common page size (436)

**A. 4KB**

B. 64KB

C. 1MB

D. 64B

378. The page table can be so large that it itself must be paged (436)

**A. T**

B. F

379. Which structure supports virtual memory (436)

A. The value prediction table

B. The Branch target table

C. The Branch Prediction Table

**D. The Page Table**

380. Which write strategy is pretty much exclusively used by virtual memory systems (437)

**A. Write back**

B. Write through

C. Write aside

D. Buffered

381. The translation lookaside buffer is the cache for the page table (438)

A. F

**B. T**

382. If a virtual page is not found in the translation lookaside buffer, a page fault results (439)

**A. F**

B. T

383. If a virtual page is not found in the page table, a page fault results (439)

A. F

**B. T**

384. If a virtual memory system has a 32-bit virtual address and 4KB pages, how long is the virtual page number? (440)

A. 32 bits

**B. 20 bits**

C. 12 bits

D. 24 bits

385. Every page table access results in an attempt to obtain data from the cache (441)

A. T

**B. F**

386. Which sort of error is cannot be encountered on a memory reference? (443)

A. Translation lookaside buffer miss

B. Page fault

C. Cache miss

**D. Overflow exception**

387. Which capability is not required to implement virtual memory? (444)

A. Allow the user mode to see but not change, processor state.

B. Provide a way to go from kernel to user mode and back.

C. Provide at least two modes, kernel and user, for the processor to be in

**D. Hold the entire page table in main memory at once.**

388. Maintaining a separate page table for each process helps ensure security (446)

**A. T**

B. F

389. Restartable instructions are important in which kind of exception? (448)

A. Processor overflow

**B. Page fault**

C. Divide by zero

D. Power interruption

390. Unmapped memory is memory which (450)

A. Does not exist.

B. Is temporarily stored on disk.

C. the processor cannot access.

**D. Cannot have page faults,**

391. The scheme of caching disk memory in main memory is called (452)

A. Non-uniform memory.

**B. Virtual memory.**

C. Uniform memory.

D. Physical memory.

392. If a program is continuously swapping pages between memory and disk it is said to be (453)

**A. Thrashing**

B. Inconsistent

C. Optimized

D. Incoherent

393. Which is not one of the four cache/virtual memory design questions? (455)

A. Which block should be replaced?

B. Where can a block be placed?

**C. Is more memory needed?**

D. How is a block found?

394. In set-associative cache, how many comparisons are needed to check for a tag match? (456)

A. Number of blocks in cache

**B. Number of blocks in a set**

C. Number of sets in cache

D. One

395. A cache miss that occurs in a set associative or direct mapped cache but not in a fully associative cache is a (459)

A. Capacity miss.

B. Compulsory miss.

**C. Conflict miss.**

D. Coherence miss.

396. Which is not a category of cache miss? (459)

A. Conflict

B. Compulsory

C. Capacity

**D. Coherence**

397. A cache can be controlled by a(n) (461)

A. Marvelous Machine

B. Turing machine

C. Linear machine

**D. Finite state machine**

398. The essence of cache control is a set of states and \_\_\_\_\_\_\_ (465)

A. Capitals

B. statelessness

**C. Transitions**

D. Combinations

399. If in the Compare-Tag state there is a miss and the victimized block is dirty, what is the next state? (465)

A. Idle

**B. Write Back**

C. Allocate

D. Compare-Tag

400. If in the Compare-Tag state there is a miss and the victimized block is clean, what is the next state? (465)

A. Idle

B. Write Back

**C. Allocate**

D. Compare-Tag

401. In which cache controller state is a new block fetched from memory? (465)

A. Write Back

**B. Allocate**

C. Compare-Tag

D. Idle

402. For our purposes, the difference between migration and replication is (467)

A. Replication is moving data to a single location, migration is moving the same data to multiple locations

**B. Migration is moving data to a single location, replication is moving the same data to multiple locations**

C. Migration causes coherency problems, Replication does not

D. Birds migrate, viruses replicate

403. When a cache controller monitors the memory bus to determine if it has valid copies of data from memory, the process is called (468)

**A. Snooping**

B. Spying

C. Monitoring

D. Checking

404. If cache controller A determines that controller B has issued a write to a memory location for which cache A holds a block, what does controller A do? (470)

**A. Invalidates the block**

B. Invokes an interrupt

C. Raises a coherency flag

D. Inserts a stall into the pipeline

405. RAID disk storage schemes are popular primarily because they (470)

A. are more dependable

B. cost less

C. have more space

**D. consume less power**

406. The Intel Core i7 processor has a 48-bit virtual address and a 44-bit physical address. How much RAM (main memory) can this processor use? (471)

A. 1 TB

B. 256 TB

**C. 4 GB**

D. 16 TB

407. A key difference between the ARM Cortex A8 and the Intel Core i7 processors is (471)

A. The i7 has two TLBs, the A-8 has three.

B. The A-8 has a larger physical address space.

**C. The i7 has four cores, the A-8 one.1**

D. The i7 consumes less power than the A-8

408. The non-blocking cache of the i7 processor allows it to (472)

**A. Process memory requests while servicing a cache miss.**

B. Does not throw an exception if there are two writes to the same block of memory

C. Adjust cache block size in real time

D. Read in variable-length blocks of memory

409. The A-8 L3 miss rate for SPEC integer benchmark programs is (474)

A. Depends on the program being run

B. Lower than for the i7 because of its relatively larger L2 ache size

C. Higher than for the i7 because of its small L3 cache size

**D. Non-existent because the A-8 has no L3 cache**

410. The design of a high-eprformance matrix multiply routine depends on knowledge of (475)

A. Number of levels of cache

B. Disk access time

C. Size of main memory

**D. Cache sizes**

411. In the multiprocessor environment of the last 10 years (502)

A. Data warehouse applications don't have the parallelism needed.

B. Manufacturers long for the uniprocessor days.

C. Energy efficiency is no longer important.

**D. Ideally, performance should scale with the number of processors.**

412. A common feature of software written for multiple processors is that it allows for processors to fail (502)

A. F

**B. T**

413. A program which can be split into multiple, independent tasks features (502)

A. Robustness

B. Dependability

**C. Task-level parallelism**

**D. Process-level parallelism**

E. Instruction-level parallelism

F. Request-level parallelism

G. Data-level parallelism

414. A set of computers connected with a local area network which all work on the same task are called a(n) (502)

A. Network

B. Grid

**C. Cluster**

D. Group Computing Infrastructure

E. Pod

F. Group

415. A shared memory processor is (503)

A. A computer that controls other computers to solve a problem

B. A processor which can access the memory of other machines

**C. A parallel processor with a single address space**

**D. Multiple processors addressing the same memory.**

E. Inefficient for solving current programming problems.

F. A processor that does not have its own memory

G. A non-uniform memory access processor.

416. A serial program can run on a parallel processor (503)

**A. T**

B. F

417. Parallel programs can run equally well on serial processors (503)

A. T

**B. F**

418. Now that we have parallel processors, what's the problem? (504)

**A. Not every problem is easily parallelized.**

B. They take up too much power.

C. Disk storage is not speeding up as quickly.

D. Main memory is still expensive.

E. Inability of networks to keep up with the demand.

**F. Lack of software that can effectively use the hardware.**

G. Their caches are not large enough.

419. A programming problem, half of which is parallelizable can be sped up five times with enough processors (506)

**A. F**

B. T

420. Effective use of multiple processors requires (508)

**A. Sharing the work effectively.**

**B. Load balancing**

C. More memory

D. Compilers which haven't yet been written.

E. Better debuggers.

F. Patience

G. Larger power supplies

421. Partitioning a 128-bit register so that it handles four single-precision floating point calculations at once is an example of (510)

A. Multiple Instruction Multiple Data

B. Multiple issue.

C. Single Instruction Single Data

D. Scalar processing

E. Multiple Instruction Single Data

**F. SIMD**

**G. Single Instruction Multiple Data**

422. Vector processing can reduce code for vector and matrix manipulations by a factor of about (512)

A. Fifty

B. 10

C. There is no reduction.

D. 1000

**E. 100**

**F. A hundred.**

G. 2

423. The essence of writing vector instructions in certain situations is to leverage (512)

A. Thread-level parallelism

B. Instruction-level parallelism

**C. SIMD**

**D. Data-level parallelism**

E. Program-level parallelism.

F. Request-level parallelism

G. Task-level parallelism

424. Single instruction, multiple data applications operate similarly to vector applications with the exception that (513)

A. They have much faster memory access.

B. Vector processors suffer when they operate on fewer elements than the vector length

C. SIMD applications use very wide registers.

**D. They cannot use strided or indexed memory access.**

E. They consume more power.

F. SIMD applications use more sophisticated memory access techniques.

**G. They use much narrower registers (not as wide).**

425. The concept of "lanes" in vector processing is (515)

A. Channeling the right operand to the right floating-point unit

B. An ineffective substitute for reducing latency.

**C. Adding more hardware to do operations in parallel**

D. Efficient, but not cost-effective for most applications.

E. Similar to reservation stations in scalar processing

F. Causing memory access to become an issue.

**G. Allocating the processing workload among several sets of functional units.**

426. Which is the most efficient use of the processor? (517)

A. Avoiding data stalls via forwarding.

B. Fine-grained multithreading

**C. Simultaneous Multithreading**

D. Superscalar multithreading

**E. The ability to issue instructions from different threads in the same cycle.**

F. Course-grained multithreading

G. Non-Uniform Memory Access.

427. A significant challenge in having multiple cores in a processor is (519)

A. Maintaining cache coherence

B. Using snooping protocol

C. Keeping them from getting too hot.

**D. Using them.**

428. What is the process of coordinating the behavior of two or more processes which may be running on different processors? (520)

A. Parsing

**B. Synchronization**

C. Snooping

D. Packaging

E. Clustering

F. Multitasking

429. A process which produces a single result from multiple data, decreasing the size of the problem is a(n) (521)

A. Oracle

B. Parallelization.

C. Miracle

D. Strip mining.

**E. Reduction**

F. Mapping

430. The opposite of symmetric multiprocessing is (523)

**A. Where main memory is not as quickly accessible by some processors.**

B. Single Instruction Multiple Data (SIMD)

C. Fine-grained multithreading.

D. Coarse-grained multithreading.

E. Vector processing

F. Simultaneous multithreading (SMT)

**G. Non uniform memory access (NUMA)**

431. Cores are connected by (536)

**A. Network topologies**.

B. Cat-5 cable.

C. PCI express busses.

D. Switches and routers

**E. On-chip networks**

F. Ethernet networks

G. Fiber

432. Whereas a bus is a set of wires which broadcast information to all listeners, a ring is capable of multiple, simultaneous transfers (536)

**A. T**

B. F

433. The simplest on-chip interconnection system is a(n) \_\_\_\_\_\_ (536)

A. Crossbar.

**B. Data lines which all nodes listen to at once.**

C. Ring.

D. Cube.

E. Mesh.

**F. Bus**

G. PCI express interface.

434. Bisection bandwidth is (537)

A. Link bandwidth.

B. The best-case intercommunication scenario.

**C. The bandwidth between two equal parts of the processor.**

**D. The data rate across a network divided in the middle.**

E. Network bandwidth.

F. Processor bandwidth.

G. No longer an accurate measure of processor performance.

435. The number of links in a fully connected network (everything connects to everything else) scales as (537)

**A. n^2**

B. log n

C. n

D. a constant

436. The bandwidth between two equal parts of the processor is called the (537)

**A. Bisection bandwidth**

B. Network bandwidth

C. Crossbar bandwidth

D. symbol rate

437. If a network is such that its four links can handle different data simultaneously, the total bandwidth is four times the link bandwidth (537)

**A. T**

B. F

438. If a fully connected network has n nodes, how many links are there? (537)

A. nLog2(n)

B. 1/n^2

**C. n(n-1)/2**

D. n\*2

E. n/2

F. n^2

439. What is the distinguishing feature of a crossbar network? (537)

**A. The number of links is proportional to n^2.**

B. It takes up the least space on a chip.

C. It uses very little power.

**D. Any node can reach any other node in one pass through the network.**

E. Any node can reach all other nodes simultaneously

F. It requires the least hardware of all on-chip networks

G. It is essentially a double-ring network

440. Because of modern design tools, any network that can be imagined can be created in silicon. (538)

A. T

**B. F**

441. Linpack is (540)

**A. a multiprocessor benchmark suite.**

B. the name of an annual computer performance competition

C. A uniprocessor test suite.

D. The standard hardware configuration for a Linux machine used in benchmark testing

E. An accepted benchmark which may not be recoded to suit the processor.

**F. Linear algebra routines for multirocessors.**

G. the nickname for the open source coders working on Linux

442. In order to ensure reliable results across benchmarks run on different systems, which of the following is done? (540)

**A. The code cannot be changed.**

B. The processor architecture must be approved by the SPEC institute

**C. The data sets used by the benchmark are fixed.**

D. Results are only published in English.

E. SPEC must run the tests.

F. The code which is run must use every possible optimization provided by the hardware.

G. The test must be monitored by a certified proctor.

443. Most multiprocessor benchmark suites feature weak scaling (541)

A. F

**B. T**

444. Traditional benchmark restrictions limit performance gains to (542)

A. the benchmark and the programmer

B. cache and main memory access improvements

**C. the architecture and compiler**

D. programmers and algorithms

445. Traditional rules of benchmark performance testing cause (542)

A. Performance tests to be expensive.

**B. Performance gains to be limited to the architecture and compiler**

C. Inaccurate assessments of capabilities on older architectures

**D. Certain performance enhancements not to be tested.**

E. High accuracy in performance measurement.

F. Newer architecture to appear faster than they really are.

G. Old benchmarks not to work on modern machines

446. Which best defines arithmetic intensity? (543)

**A. The number of floating point calculations per byte of memory accessed**

B. The mission-criticality of the application

C. FLOPs/word

D. FLOPs/operand.

E. The degree to which high precision calculations are required

F. The number of floating point operations per second

**G. FLOPs/Byte/**

447. An application which reads memory extensively and only selectively performs calculations has high arithmetic intensity (543)

**A. F**

B. T

448. Which of the following features low arithmetic intensity? (543)

A. Computational fluid dynamics

B. Weather prediction

C. Applications whose performance is limited by the speed of the processor.

D. Reading a little, calculating a lot.

**E. Reading a lot, calculating very little.**

**F. Sparse matrix operations**

G. N-body astrodynamics problems

449. Which of the following features high arithmetic intensity? (543)

A. Applications whose performace is limited by the speed of memory.

B. Sparse matrix operations

**C. Reading a little, calculating a lot.**

**D. N-body astrodynamics problems**

E. Matrix multiplication

F. Matrix inversion

G. Reading a lot, calculating very little.

450. The Roofline model characterizes (544)

A. Compiler optimization

B. Graphics speed

C. Power consumption.

**D. Hardware performance limitations**

E. Disk performance

F. Energy efficiency.

451. The slanted part of the roofline performance model represents (544)

A. Network I/O limitations

B. Floating point performance limitations

**C. Where the procesor cannot get enough data to perform calculations.**

**D. Memory bandwidth limitations**

E. Arithmetic precision limitations.

F. Where the processor can't perform calculations fast enough.

G. Effects of the power wall.

452. The flat part of the roofline performance model represents (544)

A. Network I/O limitations

**B. Where the processor can't perform calculations fast enough.**

**C. Floating point performance limitations**

D. Memory bandwidth limitations

E. Where the procesor cannot get enough data to perform calculations.

F. Arithmetic precision limitations.

G. Effects of the power wall.

453. It is not unusual for the memory-bandwidth line in the roofline performance model to have two different slopes (546)

**A. F**

B. T

454. How can the horizontal portion of the roofline performance model be raised (546)

A. Adding more banks of memory

B. Interleaving load/store and floating point calculation instructions.

C. Performing multiple issue.

**D. More computing lanes.**

**E. Use a compiler that favors SIMD floating point instructions.**

F. Adding more memory

G. Increase the number of processors.

455. The roofline model of a processor with a larger number of cores than another processor (546)

A. shows greater power consumption

B. Shows more significant memory limitations.

C. Does not show performance gains over a uniprocessor.

**D. Can perform more FLOPs/Sec**

E. Shows that memory is used more efficiently

**F. shows an extended memory bandwidth limitation line and a higher GFLOPS limit**

G. Shows that the processor may more quickly overheat

456. The units for arithmetic intensity are (548)

**A. FLOPS/Byte**

B. FLOPS/watt

C. GFLOPS/Sec

**D. Floating point operations per byte of memory read.**

E. Cycles per instruction

F. Bytes/Sec

G. GB/sec

457. The vertical axis of the roofline model is (548)

**A. GFLOPS/Sec**

B. Linear.

C. Quadratic

D. FLOPS/Byte

E. Bytes/Sec

**F. Floating point operations per second.**

G. Cycles per instruction

458. Weak scaling algorithms are likely to artificially drive up the peak GFLOP performance of a processor (549)

**A. T**

B. F

459. In digital circuits, logic blocks are organized into two types (B-04)

A. void and non void

B. Asserted and Unasserted

**C. Combinational and Stateful**

**D. Stateful and Combiational**

E. AND and OR

F. On and Off

G. High and low

460. Which concepts are most closely related? (B-04)

A. Logical OR and multiplication

**B. Truth tables and read-only memories**

C. Addition and the logical AND

D. Assert and false

E. True and deassert

F. Read-only memories and logic equations

**G. truth tables and logic equations**

461. A logic system whose blocks do not contain memory and hence compute the same output given the same input. (B-05)

**A. Combinational**

**B. Combinational logic**

C. Dubious logic

D. Sequential logic

E. Organizational logic

F. Parallel logic

G. Stateful logic

462. A group of logic elements that contain memory and hence whose value depends on the inputs as well as the current contents of the memory (B-05)

**A. Sequential**

**B. Sequential logic**

C. Amnesic logic

D. Organizational

E. Combinational logic

F. Ordinal

G. Parallel logic

463. Truth tables always describe all possible input states (B-05)

**A. F**

B. T

464. The basic boolean algebra operators are (B-06)

A. Equal and Not Equal

**B. And, Or and Not**

**C. &, |, ~**

D. If, And and But

E. &, | ^

**F. , / %**

G. Or, Nor and Xor

465. The basic component of the logic block circuit is the (B-08)

A. door

B. conductor

**C. Gate**

D. Fence

E. Path

F. Drain

**G. and/or/not gates**

466. All logic circuits can be constructed with and, or and \_\_\_\_ gates (B-08)

A. Combinational

B. Stateful

C. Stable

D. memory

E. water

**F. Inverting**

**G. not**

467. An inverted AND is a(n) (B-08)

A. additional gate

B. NOT

**C. nand**

D. Inclusive gate

E. Exclusive gate

F. NOR

**G. NAND**

468. An inverted OR is a(n) (B-08)

A. Inclusive gate

B. Exclusive gate

C. NAND

**D. NOR**

**E. nor**

F. additional gate

G. NOT

469. Almost all digital circuits can be represented with (B-08)

A. Multiplexors

**B. AND, OR and NOT gates**

C. Addition and Subtraction

D. Asserts and deasserts

E. Arithmetic logic units

F. Flip flops

**G. OR, NOT nad AND gates**

470. A digital circuit which reproduces a truth table is an example of \_\_\_\_\_\_ logic (B-09)

A. Mealy

B. Convoluted

C. Stateful

**D. Combinational**

E. Moore

F. Truthful

471. A combinational logic circuit which has n inputs and 2^n outputs is a (B-09)

A. Recoder

**B. Decoder device**

C. Processor

**D. Decoder**

E. Recorder

F. Encoder

G. Register

472. A multiplexor can be built from three gates: (B-10)

A. Three NAND gates

B. An OR and two inverters

C. two NORs and a NAND

D. Two OR gates and an AND gate

E. Three NOR gates

**F. an OR gate and two AND gates**

**G. Two AND gates and an OR gate**

473. Which circuit element selects one of a number of inputs depending on a control signal? (B-10)

A. AND gate

B. Flip-flop

C. Moore machine

D. Register

E. Arithmetic Logic Unit

**F. Multiplexor**

474. In logic, a sum is equivalent to a(n) (B-11)

**A. or**

B. NOR

**C. OR**

D. xand

E. xor

F. NAND

G. AND

475. In logic, a product is equivalent to a(n) (B-11)

A. NAND

**B. and**

C. OR

**D. AND**

E. xand

F. xor

G. NOR

476. A hardware device that implements a logical sum of products is the (B-12)

A. redundant array

B. Combinational Logic Block

**C. PLA**

D. Field Programmable Gate Array

E. Sequential block

**F. Programmable Logic Array**

G. Stateful Logic Block

477. A circuit that takes a set of input bits and produces a prestored set of output bits is a(n) (B-14)

A. Programmable Gate Array

**B. Read Only Memory**

C. Cache Block

D. Programmable Logic Array

E. Register

**F. ROM-Read Only Memory**

G. Combinational logic block

478. The difference between a Programmable Logic Array (PLA) and a Read Only Memory (ROM) is (B-15)

A. The PLA retains its ability to function after the power has been cycled

**B. The ROM does not scale well.**

C. PLAs are not efficient at handling large numbers of input lines.

D. The PLA produces a wider variety of outputs

E. The ROM requires logic to translate the inputs to outputs

**F. The ROM can reproduce any pattern of outputs with no increase in circuit complexity.**

G. The PLA does not scale well.

479. An unused output or input is called a(n) (B-17)

A. Waste of time and space

B. insignificant input or output.

C. Degree of freedom

D. Never mind.

**E. Don't Care**

F. Unused output or input

**G. Input or output don't care**

480. The purpose of a Karnaugh Map is to (B-18)

A. Program a Programmable Logic Array

B. Produce truth tables from boolean algebra

C. Program a Field Programmable Gate Array

**D. derive a boolean expression from a truth table.**

E. Determine whether or not two truth tables are the same

**F. Aid in reducing a truth table to boolean algebra**

G. Map inputs to outputs

481. In logic design, a set of data lines that is treated as a single logical signal is a(n) (B-19)

**A. Bus**

B. Poor circuit design because of the difficulty in routing the data on the chip.

C. Circuit

D. Path

**E. Set of lines with multiple sources and uses**

F. Loop

G. Trace

482. Which is an example of a hardware description language (B-20)

**A. Verilog**

B. Verisign

C. VLSI

**D. VHDL**

E. Logicore

F. Forth

G. Assembly language

483. Verilog and VHDL are examples of (B-20)

A. memory chip manufacturers.

B. motherboard manufacturers.

C. Internet security companies

**D. Software descriptions of hardware.**

**E. hardware description languages.**

F. cache designs.

G. ALU designs.

484. A computer-aided design program that can generate a gate level design based on behavioral descriptions of a digital system is a(n). (B-21)

A. Structural specifier

**B. Way of transforming behavior patterns into hardware**

C. Verifier

D. Programmable Logic Programmer

E. Goal of current research

**F. Hardware synthesis tool**

G. Behavioral specifier

485. The MIPS processor logic could be expressed in Verilog (B-23)

A. F

**B. T**

486. In order to assure proper sequencing and timing of operations, Verilog uses a process called (B-24)

A. Synchronization

B. Forking

C. Coalescing

D. Locking

**E. blocking**

F. Flow

**G. Blocking**

487. Which is not a building block of an Arithmetic Logic Unit (B-26)

**A. Outputs**

B. Multiplexors

C. One-bit adders

D. OR gates

**E. Inputs**

F. AND gates

G. Inverters

488. Addition, subtraction, logical ANDs and ORs are performed by the (B-26)

A. Shift Register

**B. Arithmetic Logic Unit**

C. Cache

D. Multiplexor

E. Sign extender

**F. ALU**

G. Register File

489. A 1-bit ALU (B-26)

A. Does not scale well to 32 bits.

B. Is low-powered enough to be used in mobile devices.

C. Is built as an academic exercise, but has no practical use.

**D. Is the building block for the MIPS 32-bit ALU.**

490. The design for a 32-bit Arithmetic Logic Unit is based on (B-27)

A. Eight input lines and eight output lines

**B. 32 1-bit ALUs**

C. 32 multiplexors

D. A read-only memory

**E. Multiple 1-bit ALUs**

F. 1-bit ALUs acting in parallel

G. 32 AND gates and 32 OR gates

491. A one-bit adder could be implemented with a read-only memory having (B-27)

A. Four inputs and three outputs

B. Two inputs and two outputs

C. An input and an output

**D. Two outputs and three inputs**

**E. Three inputs and two outputs**

F. Five control lines

G. Three inputs and three outputs

492. What signals connect 1-bit adders together so that they can form 32-bit adders? (B-27)

**A. Carry-in and carry-out**

B. Control lines

**C. The carry signals**

D. result lines

E. Overflow and underflow

F. data in and data out

G. add and subtract

493. The truth table for a one-bit adder has two data inputs and a carry input. How many rows are needed in the truth table? (B-27)

A. One

B. Sixteen

**C. 8**

D. Two

E. 32

F. Four

**G. Eight**

494. How many combinations of Data A, Data B and Carry In produce a carry out signal? (B-28)

A. 16

B. 32

C. One

**D. 4**

E. Eight

**F. Four**

G. Two

495. If A and B are adder inputs and Ci is the carry-in signal, which statement represents the result? (B-28)

A. Ci & (A | B) | A & (Ci | B) | B & (Ci | A)

B. ~Ci & A & B | Ci & ~A & B | Ci & A & B | Ci & A & B

C. Ci & A | Ci & B | A & B

**D. R = Ci & A & B | Ci & ~A & ~B | ~Ci & A &~ B | ~Ci & ~A & B**

496. Which is not a 1-bit ALU input or output (B-29)

A. Input A

**B. Chip enable**

C. Result

**D. Select**

E. Carry out

F. Operation

G. Carry in

497. Under what situation is the least-significant carry-in set to 1 and is Data B inverted? (B-30)

A. Performing ones-complement arithmetic

**B. Negating a number with twos-complement**

C. Subtracting A from B

**D. Subtracting B from A**

E. When multiplying numbers

F. Finding the next value of the program counter

G. Performing long division

498. Twos-complement arithmetic is used because (B-30)

A. Computer engineers do everything the hard way.

**B. The logic more easily translates to gates**

C. It was the first design and it worked well.

D. Speed is critical.

E. It can be manufactured under less demanding conditions.

**F. Its circuits are the simplest.**

G. It consumes the least amount of power.

499. What four functions are performed by every arithmetic logic unit (B-30)

A. Zero, result, compare, control

**B. AND, OR, add, subtract**

C. Add, subtract, multiple, divide

D. AND, OR, IF, NOT

**E. Add, subtract, AND, OR**

F. Add, subtract, branch, jump

G. Add, invert, AND, OR

500. Not (A OR B) equals (NOT A AND NOT B) (B-31)

**A. T**

B. F

501. If a < b and we perform the operation (a-b) the final one-bit adder's carry out will be (B-34)

**A. One**

**B. Asserted**

C. Indeterminate

D. Upset

E. Don't care

F. Deasserted

G. Zero

502. If a 32-bit adder performs the operation (a-b) and the bit-31 carry out is zero, what is true (B-34)

A. a < b

**B. a >= b**

C. a > b

**D. b <= a**

E. a !=b

F. a <= b

G. This will never happen

503. What method is typically to test (a == b)? (B-35)

A. Perform (a + b) and see if the result is 1

B. Perform (a + b) and see if the result is 0

**C. Negate b, add to a, see if the Zero output is asserted**

**D. Perform (a - b) and see if the result is 0**

E. Perform (a - b) and see if the result is 1

F. Branch on not equal and see if the branch is taken.

G. Branch on equal and see if the branch is taken.

504. To check if 32 bits are all zero, what is typically done? (B-35)

**A. OR the bits and invert the output.**

B. Invert the bits and AND them.

C. ADD 1 and see if the result is still 1.

D. AND the bits and invert the output.

E. ADD 1 and see if the result is still 0.

F. Invert the bits and OR them.

**G. Invert the output of all the bits ORed together**

505. What slows down the speed of a 32-bit adder? (B-38)

A. The complexity of the process.

B. Memory bus transfer time.

C. The clock speed.

D. The magnitude of the input variables.

**E. The time it takes to calculate the carry bit for each one-bit adder.**

**F. Ripple carry**

G. Parity checks.

506. Unlike software, hardware can execute \_\_\_\_\_\_\_ (B-38)

A. reliably

B. correctly

**C. at the same time**

**D. In parallel**

E. under adverse conditions

F. when powered off

G. more accurately

507. The carry out signal for a 1-bit ALU with inputs A, B and carry in (C) is expressed by (B-39)

**A. (A&B) | (B&C) | (A&C)**

B. (A&C) | (B&C)

C. (A|B) & (A|C) & (B|C)

**D. (A&B) | (A&C) | (B&C)**

E. (A|C) & (B|C)

F. A & B & C

G. A | B | C

508. If A and B are adder inputs and Ci and Co are carry-in and carry-out respectively, which statement correctly computes Co? (B-39)

A. Ci | B | A

B. Ci & A & B

**C. Ci & A | Ci & B | A & B**

D. Ci & (A | B) & A & (Ci | B) & B & (Ci | A)

509. If we build a four-bit adder with carry look ahead logic, what will be the case? (B-40)

A. The hardware will be prohibitively expensive.

**B. The circuit can be a building block for a faster 32-bit adder**

C. The circuit can provide more functions

D. The circuit is easier to build

**E. The ALU circuits will consume more power**

F. We cannot speed up adds because we need to add 32 bits.

G. The circuit will consume less power

510. Carry look-ahead is often done in group of \_\_\_\_ bits (B-45)

A. 8-10

**B. Four**

**C. 4**

D. Two

E. Six

F. 16

G. 8

511. The speed advantage of carry lookahead can be roughly obtained by counting and comparing (B-46)

**A. Gate delays**

B. The number of input bits

C. The number of times a carry signal is asserted

D. The number of OR gates

E. The number of AND gates

**F. The maximum number of gates a signal passes through from input to output**

G. The number of negations (NOTs)

512. The amount of time it takes an AND or an OR to execute is (B-46)

A. the clock skew

B. the result time

C. the circuit lag

D. related to accuracy

**E. the gate delay**

**F. about the same**

G. proportional to power consumption

513. Edge triggering is (B-48)

**A. When state-change is triggered by the voltage change in a clock pulse.**

**B. When the clock edge signals state change**

C. Ineffective at low clock frequencies.

D. Ineffective at high clock frequencies.

E. Phase gated

F. no longer used in chip-level logic

G. Sequential

514. Clock pulse edges affect (B-49)

**A. When the state is read or written.**

B. When the result is ready

C. How fast carries happen

D. When logic becomes invalid.

**E. When memory is read or written.**

F. When data moves across the data lines

G. The speed of combinational logic.

515. Reading and writing on opposite clock-cycle edges (B-50)

A. Is a more secure approach to chip design.

B. Lowers power consumption

C. Increases power consumption

D. Significantly increases circuit complexity

**E. Can be done only with operations that take less than a clock cycle.**

**F. Decreases pipelining overhead**

G. Used for instructions which cannot complete in one clock cycle.

516. Flip-flops and latches are the building blocks of (B-50)

A. Foreign policy

B. Inverters

C. AND and OR gates

D. Clocks

**E. Memory**

**F. Circuits which hold state.**

G. Arithmetic Logic Units

517. A flip-flop changes state (B-51)

A. When necessary

**B. On the clock edge**

**C. After the input changes**

D. Whenever inputs change

E. On clock failure

F. When it is enabled

G. When its state is read.

518. A latch can change state on the falling clock edge (B-51)

**A. F**

B. T

519. The values of all 32 MIPS registers are constantly being output. How do we read a register? (B-55)

A. A read signal is supplied to the desired register.

B. A clock cycle is supplied to the desired register.

**C. a 32-bit multiplexor selects the register.**

**D. A decoder determines which register's output is selected.**

E. By selecting the time at which the register is read

F. A write signal is supplied to the desired register.

G. By changing the phase of the input signal.

520. Storing data for 32 32-bit registers requires (B-55)

**A. 1024 bits**

B. 64 clock cycles

C. 512 flip-flops

D. 16 clock cycles

**E. One kilobit of SRAM**

F. significant power

G. A kilobyte of space.

521. Muxes in the register file choose which register's data will be sent to the "Read Data" outputs. How many bits wide are the conrol lines for these muxes? (B-55)

**A. 5**

B. 32

C. 1

D. 4

522. What logic circuit is used to write data to the register file? (B-56)

A. A shift register

**B. AND gates**

**C. A decoder**

D. OR gates

E. A flip-flop

F. Voltage regulators

G. An encoder

523. A static RAM has 4M 8-bit entries. How many input address lines does it have? (B-58)

A. 24

**B. 22**

C. 18

**D. Twenty two**

E. 32

F. 12

G. 8

524. In a 32-bit MIPS system, SRAM chips often store all 4 bytes of a word on the same chip (B-58)

**A. F**

B. T

525. Because SRAM chips have many memory locations which are output on a single line, an output multiplexor scheme similar to the register file design is used (B-60)

**A. F**

B. T

526. How do synchronous SRAMs and Synchronous DRAMS different from their asynchronous counterparts> (B-60)

A. They do not need to enable chip read

**B. They transfer multiple data bits at once.**

C. They use higher clock speeds to transfer more data.

D. They use critical-word-first access strategies.

**E. They use the clock pulse to speed memory transfer**

F. They use lower voltages.

G. The memory buses are wider

527. Static RAM does not require refresh cycles which DRAM does. For this reason, it consumes more power and is faster (B-63)

A. F

**B. T**

528. DRAMs store bit state in a capacitor, requiring less power than SRAM, but requiring the state be periodically refreshed (B-64)

A. F

**B. T**

529. Error correction requires multiple bits while error detection requires only one (B-66)

**A. T**

B. F

530. A state machine is a combinational logic device (B-67)

A. T

**B. F**

531. A finite state machine uses sequential logic (B-67)

A. F

**B. T**

532. The logic which reads and writes bits of memory in response to inputs is typically modeled as a finite state machine (B-67)

A. T

**B. F**

533. A traffic light which switches state regardless of the presence of cars at the stop lines is an example of a(n) (B-68)

**A. AAction based only on time**

B. Mealy machine

C. NP-Complete problem

D. Mindless policy.

E. Turing machine

**F. Moore machine**

G. Mean machine

534. A traffic light which switches state based on the presence of cars at the stop lines is an example of a(n) (B-68)

**A. Combinational logic circuit**

B. Turing machine

C. Stateful logic machine.

D. Moore machine

E. Mean machine

**F. Mealy machine**

G. Data storage circuit

535. The two types of timing logic are (B-72)

**A. Level-triggered ad edge-triggered**

B. High- and low-triggered

**C. Edge-triggered and level-triggered**

D. Level triggered and pre-triggered.

E. Edge-triggered and pre-triggered

F. Asserted and deasserted.

G. Edge-triggered and post-triggered

536. Clock skew is characterized by (B-74)

**A. the length of time it takes clock signals to arrive at different components.**

**B. Clock pulses arriving at multiple locations at different times**

C. Unequal rise times in adjacent clock pulses.

D. Voltage variations in the height of the clock pulse.

E. Excessively warm memory chips.

F. The power required to run the clock.

G. relativistic effects due to the speed of the machine.

537. What is an example of clock skew? (B-74)

A. One circuit completes its calculation before another

B. How input voltage affects clock frequency

C. A biphase clock signal where one rising edge is behind another

**D. Clock signals arriving at different circuits at different times**

E. The fact that clock periods aren't always the same length

F. Change in clock speed with CPU temperature

**G. Difference in time of arrival of the rising clock edge at different CPU circuits**

538. If a synchronous signal is not sampled at the proper time what can characterize the output? (B-76)

**A. An indeterminate state**

B. Metastatic state

C. Uncorrelated state

**D. Metastability**

E. Metaphysical state

F. Metaphorical state

G. Instability

539. The chief difference between a programmable logic device (PLD) and a field programmable gate array (FPGA) is (B-78)

A. The PLD bas both memory and logic.

**B. The PLD is combinational while the FPGA is stateful.**

**C. The FPGA has memory.**

D. PLDs are stateful circuits.

E. FPGAs are smaller.

F. The PLD cannot be programmed in the field.

G. FPGAs are combinational circuits

540. Field Programmable Gate Arrays are programmed (B-78)

**A. By establishing or breaking connections between devices**

**B. by fusing small wires together inside the device.**

C. Each time the device is powered up.

D. by field technicians.

E. By loading programs into the device's memory.

F. through use of flash memory.

G. by photo-etching.

Answers

319. A

320. B

321. C

322. A

323. A

324. A

325. D

326. B

327. B

328. D

329. B

330. B

331. A

332. C

333. C

334. C

335. D

336. B

337. A

338. D

339. D

340. B

341. B

342. B

343. D

344. B

345. D

346. D

347. A

348. D

349. B

350. D

351. B

352. D

353. D

354. A

355. A

356. A

357. D

358. C

359. B

360. A

361. C

362. D

363. A

364. B

365. B

366. B

367. B

368. B

369. D

370. A

371. B

372. A

373. A

374. B

375. C

376. B

377. A

378. A

379. D

380. A

381. B

382. A

383. B

384. B

385. B

386. D

387. D

388. A

389. B

390. D

391. B

392. A

393. C

394. B

395. C

396. D

397. D

398. C

399. B

400. C

401. B

402. B

403. A

404. A

405. A

406. D

407. C

408. A

409. D

410. D

411. D

412. B

413. C, D

414. C

415. C, D

416. A

417. B

418. A, F

419. A

420. A, B

421. F, G

422. E, F

423. C, D

424. D, G

425. C, G

426. C, E

427. D

428. B

429. E

430. A, G

431. A, E

432. A

433. B, F

434. C, D

435. A

436. A

437. A

438. C

439. A, D

440. B

441. A, F

442. A, C

443. B

444. C

445. B, D

446. A, G

447. A

448. E, F

449. C, D

450. D

451. C, D

452. B, C

453. A

454. D, E

455. D, F

456. A, D

457. A, F

458. A

459. C, D

460. B, G

461. A, B

462. A, B

463. A

464. B, C, F

465. C, G

466. F, G

467. C, G

468. D, E

469. B, G

470. D

471. B, D

472. F, G

473. F

474. A, C

475. B, D

476. C, F

477. B, F

478. B, F

479. E, G

480. D, F

481. A, E

482. A, D

483. D, E

484. B, F

485. B

486. E, G

487. A, E

488. B, F

489. D

490. B, E

491. D, E

492. A, C

493. C, G

494. D, F

495. D

496. B, D

497. B, D

498. B, F

499. B, E

500. A

501. A, B

502. B, D

503. C, D

504. A, G

505. E, F

506. C, D

507. A, D

508. C

509. B, E

510. B, C

511. A, F

512. E, F

513. A, B

514. A, E

515. E, F

516. E, F

517. B, C

518. A

519. C, D

520. A, E

521. A

522. B, C

523. B, D

524. A

525. A

526. B, E

527. B

528. B

529. A

530. B

531. B

532. B

533. A, F

534. A, F

535. A, C

536. A, B

537. D, G

538. A, D

539. B, C

540. A, B